In The Claims:

This list of claims will replace all prior versions and listings of claims in the application. Please amend the claims as set forth below.

1. **(Currently Amended)** An I/O compression test circuit for compression testing data loaded on a plurality of global I/O lines, comprising:

a plurality of test blocks for testing a plurality of global I/O line groups depending on a test block enable signal synchronously with a first strobe signal, wherein the plurality of global I/O lines are divided into the plurality of global I/O line groups;

a decision block for deciding a test result in response to output signals from the plurality of test blocks;

a driving block for driving ~~outputting a test result signal in response to~~ a decision signal outputted from the decision block synchronously with a second strobe signal; and

a control block for generating the first strobe signal, a reset signal, and the second strobe signal depending on a compression test enable signal and a global I/O line strobe signal, wherein the reset signal initializes ~~controlling a test timing of the test blocks, initializing~~ an input terminal of the decision block ~~and controlling a driving timing of the driving block~~, wherein the global I/O line strobe signal is activated when data are loaded on the global I/O lines.

2. **(Currently Amended)** The circuit according to claim 1, wherein the test ~~block comprises~~ blocks comprise:

a logic means for performing a logic operation on [[a]] the compression test enable signal, [[a]] the test block enable signal and the first strobe signal ~~a test timing control signal~~;

a first test means for outputting a first level when at least one of data transmitted into the global I/O line group is at a different level depending on an output signal from the logic means; and

a second test means for outputting a second level when at least one of data transmitted into the global I/O line group is at a different level depending on an output signal from the logic means.

3. **(Original)** The circuit according to claim 2, wherein the decision block comprises:

a first input terminal connected in common to an output terminal of the first test means of the test block;

a second input terminal connected in common to an output terminal of the second test means of the test block;

a first transmission means for selectively transmitting a potential of the first input terminal depending on a potential of the second input terminal; and

a second transmission means for selectively transmitting a signal having an inverted potential of the first input terminal depending on a potential of the second input terminal.

4. **(Original)** The circuit according to claim 3, wherein the decision block further comprises:

a first latch means for maintaining a potential of the first input terminal; and

a second latch means for maintaining a potential of the second input terminal.

5. **(Currently Amended)** The circuit according to claim 3, wherein the decision block further comprises:

a first initialization means for selectively initializing a potential of the first input terminal to the first level depending on [[an]] the reset signal outputted from the control block; and

a second initialization means for selectively initializing a potential of the second input terminal to the second level depending on the reset signal.

6. **(Currently Amended)**The circuit according to claim 1, wherein the driving block comprises:

a transmission means for selectively transmitting ~~an driving control~~ the decision signal outputted from the decision block synchronously with ~~respect to an output signal~~ the second strobe signal from the control block; and

a driving means for pulling up or down an output terminal in response to ~~a signal~~ the decision signal selectively transmitted by the transmission means.

7. **(Original)** The circuit according to claim 6, wherein the driving block further comprises a latch means for maintaining a potential of the output terminal.

8. **(Currently Amended)**The circuit according to claim 1, wherein the control block comprises:

a first strobe signal generator for generating [[a]] the first strobe signal in response to [[a]] the compression test enable signal and ~~a detecting~~ the global I/O line strobe signal, ~~wherein the strobe signal controls a test timing of the test timing, wherein the detecting signal is activated when data are loaded on the global I/O line~~;

~~an initialization~~ a reset signal generator for generating ~~an initialization~~ the reset signal in response to the compression test enable signal and the global I/O line strobe ~~detecting~~ signal, wherein the ~~initialization~~ reset signal initializes an input terminal of the decision block to a predetermined level; and

a ~~driving control~~ second strobe signal generator for generating ~~a driving control~~ the second strobe signal by delaying the first clock signal ~~in response to the strobe signal~~.

9. **(Currently Amended)**The circuit according to claim 8, wherein the first strobe signal generator comprises:

a logic means for performing a logic operation on the compression test enable signal and the ~~detecting~~ global I/O line strobe signal; and

a pulse generator for outputting a pulse signal in response to an output signal from the logic means.

10. **(Currently Amended)** The circuit according to claim 8, wherein the initialization signal generator comprises:

a first logic means for performing a logic operation on the compression test enable signal and the ~~detecting~~ global I/O line strobe signal; and

a second logic means for performing a logic operation on the compression test enable signal and an output signal from the first logic means.

11. **(Currently Amended)** The circuit according to claim 8, wherein the ~~driving control~~ second strobe signal generator comprises a delay means for delaying the first strobe signal for a predetermined time.